UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,432	12/15/2000	Jun Souk Joung	HI-023	8762

34610 7590 07/13/2006

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER	
DELGADO, MICHAEL A	
ART UNIT	PAPER NUMBER
2144	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,432	JOUNG, JUN SOUK	
	Examiner	Art Unit	
	Michael S. A. Delgado	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10,11,15-20 and 25-27* is/are rejected.

7)☒ Claim(s) *6-9,12-14 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/14/2006 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 10-11, 15-20 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 5,978,589 by Yoon in view of US Patent No 5,655,079 by Hirasawa et al.

In claim 1, Yoon teaches about a method for down-loading data from an upper processor to a plurality of lower processors " middle processors" of a mobile communications switching

system "base station system" in a process of resetting (processor being initialized after power source is applied) the processors, the method comprising (Col 2, lines 30-45) (Fig 2):

requesting an information download from the lower processors to the upper processor (Col 2, lines 40-50);

accessing a memory of the upper processor containing the requested information download (Col 2, lines 40-50);

but does not explicitly teach about grouping the lower processors with a representative address by creating the accessed information in a information processing code (IPC) format supported by error checking;

Yoon teaches the need to reduce the time taken to download configuration files to multiple processors in a mobile system (Col 1, lines 35-45). Yoon further teaches the need to have a completion signal to insure that the files are ready to be deployed (Col 2, lines 45-55). To be complete, it is important that the file in question is error free for the operation to be successful.

Hirasawa teaches a solution on reducing the time to download to multiple computers (each computer represent a processor) while providing means for error checking (Col 10, lines 55-65). Hirasawa teaches about creating the accessed information in an information processing code IPC format (Fig 7) (Col 4, lines 50-65);

determining whether the accessed information has an error (Col 10, lines 55-65);

transferring the IPC format information from the upper processor to the lower by using the group representative address, the transferred IPC format information including the accessed information and the group representative address (Col 7, lines 35-50) (Col 16, lines 10-20).

Hirasawa method provided an improvement approach to the downloading of code, which allowed one format to be used for group and individual download which reduces network traffic (Col 1, lines 35-45) (Col 2, lines 30-35). By allowing group downloading, the time taken to configure all the processors is less, which is the goal of Yoon.

It would have been obvious at the time of the invention for some one of ordinary skill to improve on the efficiency of Yoon invention by utilizing Hirasawa's method, which reduces the amount of network traffic that is needed when configuring devices of the same type.

In claim 2, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the resetting of the processors includes an initial loading and a re-loading (Yoon Col 2, lines 30-45).

In claim 3, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the group representative address includes all the lower processors (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

In claim 4, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping the plurality of lower processors using the group representative address (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

In claim 5, Yoon combined with Hirasawa, teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping at least one additional lower processor "lower processor" (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

In claim 10, Yoon combined with Hirasawa, teaches about a method for downloading data from a first processor to a plurality of second processors "middle processors" while resetting the processors, the method comprising (Yoon Col 2, lines 30-45) (Fig 2):

transmitting a request for an information download from the plurality of second processors to the first processor (Yoon Col 2, lines 30-45);

accessing a memory once of the first processor for the requested information (Yoon Col 2, lines 40-50);

grouping the second processors using a prescribed processor address (Covered in claim 1); and

assembling the accessed information in a prescribed format (Covered in claim 1) ; and

transferring the assembled requested information from the first processor to at least two second processors using a group representative address, the transferred assembled request information including the accessed information relating to the resetting of the processors and the group representative address (Covered in claim 1).

In claim 11, Yoon combined with Hirasawa, teaches about a method of claim 10, wherein the grouping of the plurality of lower processors is performed using the group representative address (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35).

In claim 15, Yoon combined with Hirasawa, teaches about a method of claim 10, further comprising determining whether the accessed requested information has an error (Hirasawa Col 10, lines 55-65).

In claim 16, Yoon combined with Hirasawa, teaches about a mobile communications switching method comprising (Fig 2):

requesting information from a first processor "upper processor" relating to the resetting of processors (processor being initialized after power source is applied) (Yoon Col 2, lines 30-45) (Fig 2);

grouping a plurality of second processors "middle processors" using a representative address of the plurality of second processors (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35);

providing the requested information in an information processing code (IPC) format (Covered in claim 1); and

transferring the requested information in the IPC format from the first processor to the plurality of second processors based on the representative address of the plurality of second processors , the transferred information in the IPC format including the request information relating to the resetting of the processors and the representative address of the plurality of the second processor (Yoon Col 2, lines 30-45) (Hirasawa Col 4, lines 20-35) (Covered in claim 1).

In claim 17, Yoon combined with Hirasawa, teaches about a method of claim 16, further comprising accessing a memory of the first processor (fig 1, 6) having the requested information (Yoon Col 2, lines 35-45).

In claim 18, Yoon combined with Hirasawa, teaches about a method of claim 17, further comprising determining whether the requested information has an error (Covered in claim 1).

In claim 19, Yoon combined with Hirasawa, teaches about a method of claim 16, wherein the method is provided in a process of resetting the second processors (Yoon Col 2, lines 30-45).

In claim 20, Yoon combined with Hirasawa, teaches about a method of claim 19, wherein the resetting of the second processors includes an initial loading and a re-loading (Yoon Col 2, lines 30-45).

In claim 25-26, Yoon combined with Hirasawa, teaches about a method wherein group representative address comprises an address of at least two of the lower processor (Hirasawa Col 4, lines 20-30) (Hirasawa Col 16, lines 10-20) (Covered in claim 1).

Allowable Subject Matter

1. Claims 6-9, 12-14, and 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter: prior art failed to teach about using a representative address that comprises a node address (NA), a BHIU address (BA), a cinu address (CA), and a slot address (SA).

Response to Arguments

1. Applicant's arguments include the failure of previously applied art to expressly disclose the limitation of a reset taken place prior to the downloading of information, which has the Information Processing Code (IPC) format. See Response, Remarks dated 3/06/2006, pages 9-10. It is evident from the detailed mappings found in the above rejection(s) that Yoon disclosed this functionality of an upper processor transferring information with a lower set of processors. Further, it is clear from the numerous teachings (previously and currently cited) that the provision for IPC format, was widely implemented in the networking art. Thus, Applicant's arguments drawn toward distinction of the claimed invention and the prior art teachings on this point are not considered persuasive.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,212,557 by Oran teaches about a method and apparatus for synchronizing upgrades in distributed network data processing systems.

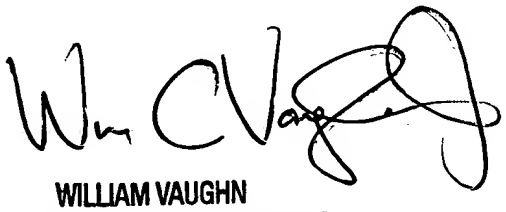
US Patent 6,021,442 by Ramanan et al, teaches about a method and apparatus for partitioning an interconnection medium in a partitioned multiprocessor computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. A. Delgado whose telephone number is (571) 272-3926. The examiner can normally be reached on 7.30 AM - 5.30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William C. Vaughn Jr. can be reached on (571)272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MD



WILLIAM VAUGHN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100